IN THE SPECIFICATION:

Please replace the paragraph at page 1, lines 11-17, with the following rewritten paragraph:

a1

To test Bit Error Ratio (BER) on all channels of a parallel optical communication transmitter, all channels must be exercised. Such testing requires equipment that includes a single data generator and data detector, and they must be switched to each input and output of a laser driver chip until all channels are tested, or in the alternative the test equipment must include multiple data generator/detectors.

Please replace the paragraph at page 1, lines 18-27, with the following rewritten paragraph:

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In an attempt to solve the problems described above, an on-chip parallel data generator, including a Built In Self Test (BIST) parallel data generator, is integrated into the transmitter so that all optical outputs may be switched synchronously. The BIST generator requires only one clock input which clocks the BIST generator for all channels. However, a problem still exists ~~that~~ because when asynchronous BER testing is desired, the electrical inputs cannot be used for any other testing since the parallel inputs of the chip are ignored during BIST operation.

Please replace the paragraph at page 5, line 24, through page 6, line 3, with the following rewritten paragraph:

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Figure 1 shows a BIST generator **5** that is incorporated into the parallel optical transmitter **100**, in accordance with an example embodiment of the present invention.

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Parallel optical transmitter **100** includes N laser driver channels Channels 0-N (**CH0-CHN**) in addition to the aforementioned BIST generator **5**.

Please replace the paragraph at page 6, lines 4-11, with the following rewritten paragraph:

An external clock source **1** may be applied to the inputs of Channel N **CHN**, during BIST mode operation. Otherwise, the Channel N inputs are data. EBIST **11** and SBIST **12** are control signal inputs used to select the type of data that is passed to the laser driver, choosing from BIST data and external data. OR gate 7 enables the BIST generator 5. Thus, when EBIST and SBIST are 0, BIST generator 5 is disabled, as will be described further below regarding Logic Block 70 in ~~Fig.~~ Figure 2. BIST Generator 5 may receive clock signals from Channel N (CHN), as shown in Figure 1, or the clock source for BIST generator 5 may be an oscillator with an arbitrarily chosen frequency.

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Please replace the paragraph at page 6, line 12 to page 7, line 4, with the following rewritten paragraph:

Figure 2 shows the contents of each channel in Figure 1. The external data inputs **20** are differential signals that are applied to the inputs of Data Receiver **50** and Signal Detector **40**. Signal Detector **40** determines if a signal with a valid common mode (average voltage) is present on the Tx inputs **20**. The Data Receiver **50** buffers the Tx inputs **20**, and the outputs **55** of Data Receiver are connected to multiplexer input A **85**. The BIST generator **5** of Figure 1 generates BIST inputs **30**, and the inputs **30** are buffered by the BIST Buffer **60**. BIST Buffer outputs **65** are connected to the multiplexer

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input B **86**. Logic block **70** controls which of inputs "A" **85** or "B" **86** is passed by multiplexer **80** to the inputs of Laser Driver **90**. Laser Driver **90** then converts the differential input to a single ended current **95** to drive the laser. Figure 2 shows, as an example, how Signal Detector **40** is connected in parallel with the Data Receiver **50** and how the output **45** of Signal Detector 40 is passed to the Multiplexer **80**.